IN THE DRAWINGS

Applicants respectfully propose to amend Figure 1 to show that the frame buffer is element 140, as shown in Figure 2 of the present application. A submission of the proposed drawing amendment containing a red-lined Figure 1 is being separately submitted concurrently with the present response.

IN THE CLAIMS

Please enter the following amendments:

Please cancel Claim 1 without prejudice.

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12. (Amended) [The computer system of Claim 1,] A computer system, comprising:

a processor for performing geometric calculations on a plurality of vertices of a primitive;

a rasterization circuit coupled to the processor that rasterizes the primitive according to a rasterization process which operates on a floating point format;

a frame buffer coupled to the rasterization circuit for storing a plurality of color values; and

a display screen coupled to the frame buffer for displaying an image according to the color values stored in the frame buffer;

wherein the rasterization circuit performs scan conversion on vertices having floating point color values.

2 3. (Amended) [The computer system of Claim 1 further comprising:] A computer system, comprising:

a processor for performing geometric calculations on a plurality of vertices of a primitive;

a rasterization circuit coupled to the processor that rasterizes the primitive according to a rasterization process which operates on a floating point format;

a frame buffer coupled to the rasterization circuit for storing a plurality of color values;

a display screen coupled to the frame buffer for displaying an image according to the color values stored in the frame buffer;

A2 CONT.

a texture circuit coupled to the rasterization circuit that applies a texture to the primitive, wherein the texture is specified by floating point values; and

a texture memory coupled to the texture circuit that stores a plurality of textures in floating point values.

Please cancel Claim 4 without prejudice.

Please cancel Claim 5 without prejudice.

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3 6. (Amended) [The computer system of Claim 5,] A computer system, comprising:

a processor for performing geometric calculations on a plurality of vertices of a primitive;

A3 a rasterization circuit coupled to the processor that rasterizes the primitive according to a rasterization process which operates on a floating point format;

a frame buffer coupled to the rasterization circuit for storing a plurality of color values; and

a display screen coupled to the frame buffer for displaying an image according to the color values stored in the frame buffer;

A3 cont.

wherein the floating point format is comprised of sixteen bits in a s10e5 format.

Please cancel Claim 7 without prejudice.

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4 ~~8~~. (Amended) [The computer system of Claim 1 further comprising] A computer system, comprising:

a processor for performing geometric calculations on a plurality of vertices of a primitive;

a rasterization circuit coupled to the processor that rasterizes the primitive according to a rasterization process which operates on a floating point format;

A4

a frame buffer coupled to the rasterization circuit for storing a plurality of color values;

a display screen coupled to the frame buffer for displaying an image according to the color values stored in the frame buffer; and

a fog circuit coupled to the rasterization circuit for performing a fog function, wherein the fog function operates on floating point color values.

Please cancel Claim 9 without prejudice.

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5 ~~10~~. (Amended) [The computer system of Claim 1 further comprising] A computer system, comprising:

A5

a processor for performing geometric calculations on a plurality of vertices of a primitive;

a rasterization circuit coupled to the processor that rasterizes the primitive according to a rasterization process which operates on a floating point format;

a frame buffer coupled to the rasterization circuit for storing a plurality of color values;

a display screen coupled to the frame buffer for displaying an image according to the color values stored in the frame buffer; and

a blender coupled to the rasterization circuit which blends floating point color values.

~~11~~ 9. (Amended) [The computer system of Claim 1 further comprising] A computer system, comprising:

a processor for performing geometric calculations on a plurality of vertices of a primitive;

AS CONT.

a rasterization circuit coupled to the processor that rasterizes the primitive according to a rasterization process which operates on a floating point format;

a frame buffer coupled to the rasterization circuit for storing a plurality of color values;

a display screen coupled to the frame buffer for displaying an image according to the color values stored in the frame buffer; and

logic coupled to the rasterization circuit which performs per-fragment operations on floating point color values.

~~12~~ 7. (Amended) [The computer system of Claim 1,] A computer system, comprising:

a processor for performing geometric calculations on a plurality of vertices of a primitive;

a rasterization circuit coupled to the processor that rasterizes the primitive according to a rasterization process which operates on a floating point format;

a frame buffer coupled to the rasterization circuit for storing a plurality of color values; and

A5 CONT.

a display screen coupled to the frame buffer for displaying an image according to the color values stored in the frame buffer;

wherein the processor, the rasterization circuit, and the frame buffer are on a single semiconductor chip.

A6

~~15~~ 10. (Amended) The method of Claim [13] ~~14~~ 9, wherein the floating point values are comprised of sixteen bits.

Please cancel Claim 22 without prejudice.

Please cancel Claim 23 without prejudice.

Please cancel Claim 24 without prejudice.

Please cancel Claim 25 without prejudice.

A7

~~26~~ 17. (Amended) [The method of Claim 22,] In a computer system, a method for operating on data stored in a frame buffer, comprised of:

storing the data in the frame buffer in a floating point format;

reading the data from the frame buffer in the floating point format;

operating directly on the data in the floating point format; and

writing the data to the frame buffer in the floating point format;

wherein the steps of writing, storing, and reading the data in the frame buffer in [a] the floating point format [is] are further comprised of a specification of the floating point format, wherein the specification corresponds to a level of range and precision.

A7 cont.

Please cancel Claim 31 without prejudice.

Please cancel Claim 32 without prejudice.

Please cancel Claim 33 without prejudice.

Please cancel Claim 34 without prejudice.

~~35~~ 22. (Amended) [The computer system of Claim 31,] A computer system having a floating point frame buffer for storing a plurality of floating point color values;

B8

wherein the floating point color values are written to, read from, and stored in [a] the frame buffer using a specification of the floating point color values that corresponds to a level of range and precision.
